

IN THE DRAWINGS:

Submitted herewith are replacement sheets for Figs. 4A-4D and 7A-7F incorporating revisions to label Figs. 4A-4D with the legend "Prior Art" and to remove the "Prior Art" label from Figs. 7A-7F in order to conform the drawings to the specification.

REMARKS

In the last Office Action, the Examiner rejected claim 6 under 35 U.S.C. §103(a) as being unpatentable over Figs. 7A-7F of the present application in view of U.S. Patent No. 6,541,333 to Shukuri et al. Claims 2-5 were allowed by the Examiner. Additional art was cited of interest.

Applicants and applicants' counsel note with appreciation the indication of allowable subject matter concerning claims 2-5. However, for the reasons noted below, applicants respectfully submit that independent claim 6 also patentably distinguishes from the prior art of record.

In accordance with the present response, independent claims 2 and 3 have been amended to clarify that the transistor is of a "second conductivity type" in order to conform to the conductivity type of the source and drain regions. This amendment is consistent with the disclosure in the specification and necessary since the conductivity type of a MOS transistor is the same as the conductivity type of the source and drain of the MOS transistor. Claims 2-6 have also been amended in formal respects to improve the wording and to bring them into better conformance with U.S. practice.

The Summary of the Invention (pgs. 6, 7, 9, 10) and the Detailed Description of the Preferred Embodiments (pgs. 27, 29, 31) of the specification have been suitably revised to conform to the amendments to claims 2 and 3 relating to the

second conductivity type transistor. The specification has been further revised to bring it into better conformance with U.S. practice. A new abstract which more clearly reflects the invention to which the amended and new claims are directed has been substituted for the original abstract.

Submitted herewith are replacement sheets for Figs. 4A-4D and 7A-7F incorporating revisions to label Figs. 4A-4D with the legend "Prior Art" and to remove the "Prior Art" label from Figs. 7A-7F in order to conform the drawings to the specification. More specifically, Figs. 4A-4D relate to a method of manufacturing a conventional SOI transistor, as described on pages 1-3 and 12 of the specification. Figs. 7A-7F relate to a method of manufacturing a semiconductor integrated circuit according to a second embodiment of the present invention, as described on pages 12 and 18-20 of the specification.

Applicants respectfully submit that independent claim 6 patentably distinguishes from the prior art of record.

The Examiner rejected claim 6 under 35 U.S.C. §103(a) as being unpatentable over Figs. 7A-7F of the present application in view of U.S. Patent No. 6,541,333 to Shukuri et al. Applicants respectfully traverse this rejection.

Applicants respectfully submit that the disclosure in Figs. 7A-7F of the present application is inapplicable as a

reference to reject independent claim 6 because Figs. 7A-7F relate to the structure and method of producing a semiconductor integrated circuit according to the present invention, not the conventional art. In this regard, page 12, lines 12-13 of the specification discloses that Figs. 7A-7F are process flow diagrams "showing a second manufacturing method of the present invention." Likewise, pages 18-20 of the specification describe the structure and method of manufacturing the semiconductor integrated circuit according to the second embodiment of the present invention.

In view of the foregoing, applicants respectfully request that the rejection of claim 6 under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing amendments and discussion,
the application is believed to be in allowable form.
Accordingly, favorable reconsideration and allowance of the
claims are most respectfully requested.

Respectfully submitted,

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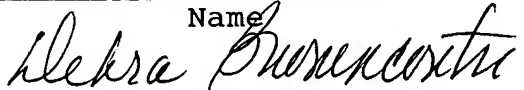
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December 19, 2005

Date